Fig. 2 is a block diagram of the modulator driver apparatus set forth in Fig. 1 for operating the modulator of an electro-optical transmission system,

Fig. 3 is a circuit diagram of components of the modulator driver limited amplifier variable amplitude apparatus set forth in Fig. 2,

Fig. 4 is a circuit diagram of one of a plurality of resistor cells of the programmable resistor array set forth in Fig. 2 for powering the linear amplifiers,

Fig. 5 is a block diagram of apparatus of the programmable resistor array set forth in Fig. 2 for selecting ones of the plurality of resistor cells set forth in Fig. 4,

Fig. 6 is a diagram of apparatus controlled by the memory cells of Fig. 5 for powering resister cells of the programmable resistor array set forth in Fig. 4, and

Fig. 7 is a circuit diagram of the modulator driver peak detector set forth in Fig. 2 for determining loss of signals for driving the electro-optical transmission system.

The logic component circuitry of the modulator driver apparatus set forth in Figs. 1 through Fig. 5 of the drawing is performed by transistors, circuit elements, peak detectors, controller units, digital-to-analog converters and central processor units, the individual operation of which are well known in the art and the details of which need not be disclosed for an understanding of the invention. Typical examples of these logic circuitry are described in numerous textbooks. For example, such types of logic circuitry, among others, are described by J. Millman and H, Taub in Pulse, Digital and Switching Waveforms, 1965, McGraw-Hall, Inc., H. Alex Romanowitz and Russell E. Puckett in Introduction to Electronics, 1968, John Wiley & Sons, Inc., E. J. Angelo, Jr. in Electronic Circuits, Second Edition, 1958, McGraw Hill, Inc. and in The TTL Data Book for Design Engineers, Second Edition, 1976, Texas Instruments Incorporated.

in response thereto modulates the light generated by light source 30 and applies the modulated light to a transmission facility or the like.

With particular reference to Fig. 2, there is shown modulator driver 10 having apparatus for use in driving modulator 20 which may be one of a number of modulators such as a lithium niobate modulator. Input information is applied along with duty cycle control information to the inputs of a hard limiting amplifier 100. The hard limiting amplifier 100 is a limited amplifier for receiving multiplexed binary data signals and for generating amplified and limited frequency output signals representative of the received multiplexed binary data signals. It performs single ended to differential signal conversion of the input information and provides a hard limiting function on the input signal. Differential and complementary outputs of the hard limiting amplifier 100 are connected to the inputs of the variable amplitude buffer 101 which generates an output signal from 0db to a minus 4db in response to the duty cycle information. The output of variable amplitude buffer is connected to the input of the linear amplifier 102 having an output connected to the input of linear amplifier 104. Programmable resistor array 103 has outputs connected to linear amplifiers 102 and 104 and is controlled by controller 105 in response to instructions from processor 50 to control the response of linear amplifiers 102 and 104 in generating an output for operating modulator 20. The output of linear amplifier 104 is applied to peak detector 106 to indicate a loss of the modulator operating signal to drive modulator 20.

Limited amplifier 100 receives the multiplexed binary data signals and generates a pair of complementary amplified and limited frequency output signals representative

high fidelity output signals with low over and undershoot and a high extinction ratio to drive the modulator 20. The gain of each stage of a linear amplifier will vary over the process of amplifying signals. The limited amplifier apparatus of processor controlled modulator driver 10 has a pair of linear amplifiers 102, 104 connected in series and which have a limited frequency response for filtering and thereby reducing the over and undershoot of signals applied by the differential amplifier components of variable amplitude buffer 101 to the input of the linear amplifier 102. A programmable resistor array 103 controlled by controller 105 in response to instructions generated by processor 50 equalizes the gain of each stage of linear amplifier 102 and 104. Programmable resistor array 103 has a plurality of resistor cells, Fig. 4, each consisting of a plurality of circuit elements 1030, 1031, 1032 and 1033 connect in parallel between voltages Vcc and Vee and each arranged to supply a processor selected a voltages Vx to linear amplifiers 102 and 104, Fig. 2.

Processor 50 controls the gain of the linear amplifiers 102 and 104 over bus 106 by instructing controller 105, via address leads A0, A1 and Cs, Fig. 5, to enable logic Dx 1030 to select ones of the memory cells 1031 through 1034. Data is then sent to the selected one of memory cells to enable the selected memory cell to control the gain of linear amplifiers 102 and 104, Fig. 2, by varying the voltage Vx of a resistor cell, Fig. 4, of the selected one of resistor arrays 1 through 4, Fig. 5 to be one of the voltages V1 through V4. The selected memory cell, Fig. 6, is instructed by the appropriate data information transmitted by processor 50 and over leads D1 and Write to operate switching logic 1035 to vary the voltage Vee supplied to the appropriate resistor cells,

a controller connected to the differential amplifier and responsive to a processor for selectively controlling the amplitude of output pulses of the differential amplifier.

6. The modulator apparatus set forth in claim 5 wherein the processor controlled modulator driver central processor unit controlled linear amplifiers comprises

a pair of linear amplifiers having a limited frequency response for filtering and thereby reducing the over and undershoot of signals applied by the differential amplifier to the input of the linear amplifiers.

7. The modulator apparatus set forth in claim 6 wherein the processor controlled modulator driver comprises

a plurality of programmable resistor arrays for supplying power to the linear amplifiers.

8. The modulator apparatus set forth in claim 7 wherein the processor controlled modulator driver comprises

memory means controlled by the controller for enabling the programmable resistor arrays to equalize gains of the linear amplifiers.

9. The modulator apparatus set forth in claim 8 wherein the processor controlled modulator driver comprises

detector means connected to the output of the linear amplifiers for detecting absence of linear amplifier generated signals as a loss of modulating signals.

10. Apparatus for driving a modulator for modulating data signals onto a light wave comprising

a limited amplifier for receiving multiplexed binary data signals and for generating amplified and limited frequency output signals representative of the received multiplexed binary data signals,

a differential amplifier connected to an output of the limited amplifier for precisely controlling the amplitude and generating a low level of over and undershoot of output signals over a wide range of the limited amplifier output signals, and

processor controlled amplifier means connected to the output of the differential amplifier for generating high fidelity output signals with low over and undershoot and a high extinction ratio for driving the modulator.

11. The modulator driving apparatus set forth in claim 10 further comprising

a processor controlled controller for enabling the differential amplifier to generate variable amplitude pulses at the output thereof.

12. The modulator driving apparatus set forth in claim 11 wherein the processor controlled amplifier means comprises

a pair of linear amplifiers having a limited frequency response for filtering and thereby reducing the over and undershoot of variable amplitude pulses generated by the differential amplifier.

13. The modulator driving apparatus set forth in claim 12 further comprising

a plurality of programmable resistor arrays for supplying power to the linear amplifiers.

14. The modulator apparatus set forth in claim 13 wherein the processor controlled driver comprises